In the Claims:

Please amend the claims as follows:

1. (Currently Amended) A computer system, comprising:

multiple processors;

a plurality of resources assigned to node groups;

a first descriptor of respective topological levels of at least one of the resources; and

a second descriptor of respective performance of said resources,

wherein the first and second descriptors are produced by firmware in a single computer system.

2. (Original) The system of claim 1, wherein said descriptor is a first level data structure, and said second descriptor is a primary data structure.

3. (Original) The system of claim 2, wherein said primary data structure comprises a pointer to a secondary data structure.

4. (Original) The system of claim 1, further comprising a node identifier for each node for identifying positional placement of a resource.

5. (Original) The system of claim 4, wherein said node identifier represents multiple levels of interconnect.

6. (Original) The system of claim 1, further comprising a dynamic updator of at least the first and second descriptors.

7. (Original) The system of claim 6, wherein said dynamic updator reflects real-time system configuration into the first descriptor.

8. (Original) The system of claim 6, wherein said dynamic updator reflects real-time system performance into the second descriptor.

9. (Previously Presented) The system of claim 1, wherein said first descriptor includes a pointer to a secondary data structure having a descriptor selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors, and share cache descriptors.

10. (Previously Presented) The system of claim 9, wherein said shared cache descriptor reflects interconnects of the system.

11. (Original) The system of claim 10, wherein said shared cache descriptor reflects latencies of the interconnects.

12. (Previously Presented) The system of claim 1, wherein said second descriptor reflects average latency between the node groups.

13. (Currently Amended) An article comprising:

a computer-readable recordable data storage medium readable by a computer having multiple processors and a plurality of resources assigned to node groups;

means in the medium for determining topological levels of at least some of the resources; and

means in the medium for determining performance of said resources,

wherein said topological level determining means and said performance determining means are capable of being stored in firmware of a single computer ~~the~~ system.

14. (Canceled) The article of claim 13, wherein the medium is a recordable data storage medium.

15. (Canceled) The article of claim 13, wherein the medium is a modulated carrier signal.

16. (Original) The article of claim 13, wherein said topological level determining means is a first descriptor and said performance determining means is a second descriptor.

17. (Original) The article of claim 13, further comprising a node identifier for identifying positional placement of a resource for each node.

18. (Previously Presented) The article of claim 16, wherein said first descriptor includes a pointer to a secondary data structure having a descriptor selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors, and share cache descriptors.

19. (Currently Amended) The article of claim 13, wherein said a shared cache descriptor reflects interconnect of resources.

20. (Original) The article of claim 19, wherein said shared cache descriptor reflects latencies of the interconnects.

21. (Previously Presented) The article of claim 16, wherein said second descriptor reflects average latencies between node groups.

22. (Currently Amended) A method for enabling allocation of resources in a multiprocessor, comprising:

assigning multiple resources into node groups; and

maintaining system resource topology and performance descriptions as at least one data structure produce by firmware in a single computer system.

23. (Original) The method of claim 22, further comprising traversing the data structure to enable allocation of at least some of the resources.

24. (Original) The method of claim 22, wherein said traversal step includes accessing a second data structure.

25. (Previously Presented) The method of claim 24, wherein said second data structure is selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors and shared cache descriptors.

26. (Previously Presented) The method of claim 24, wherein said second data structure includes a shared cache descriptor for describing at least part of a system interconnect including latency between sibling nodes.

27. (Original) The method of claim 22, further comprising maintaining at least average latency between at least two of the nodes.

28. (Original) The method of claim 22, wherein said traversal step includes recursively accessing additional data structure levels.